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WPI, EPODOC, PAJ, INSPEC

(54) Abstract Title
Improvements in or relating to fast frequency-hopping synthesisers

(57) A low noise fast frequency-hopping local oscillator for use in a base station for a mobile telephone network, in which a low noise hopping frequency is provided by a combination of a fast direct digital synthesis (DDS) circuit feeding a frequency divider, followed by a vector modulator and phase lock led loop acting together to translate the hopping frequency from a relatively low frequency range to the required RF frequency range for mobile telephone communications.

FIG 3

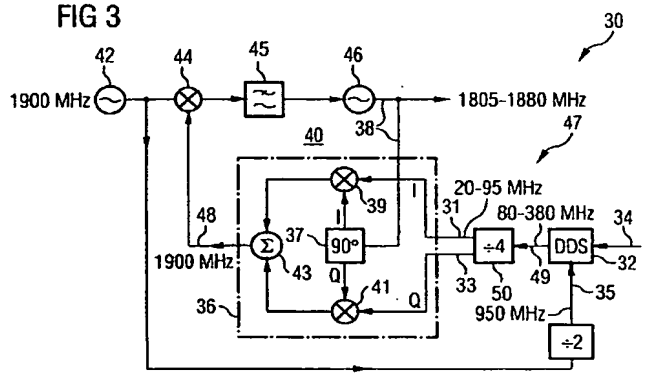
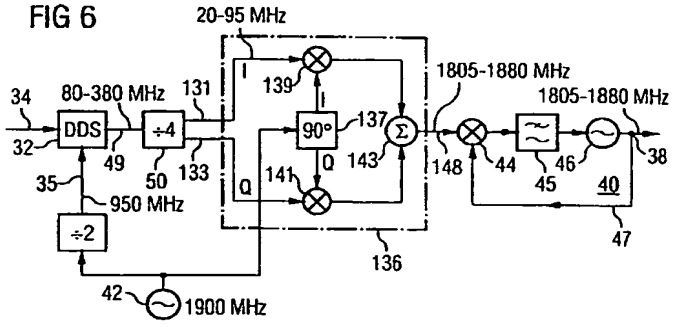


FIG 6



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

FIG 1

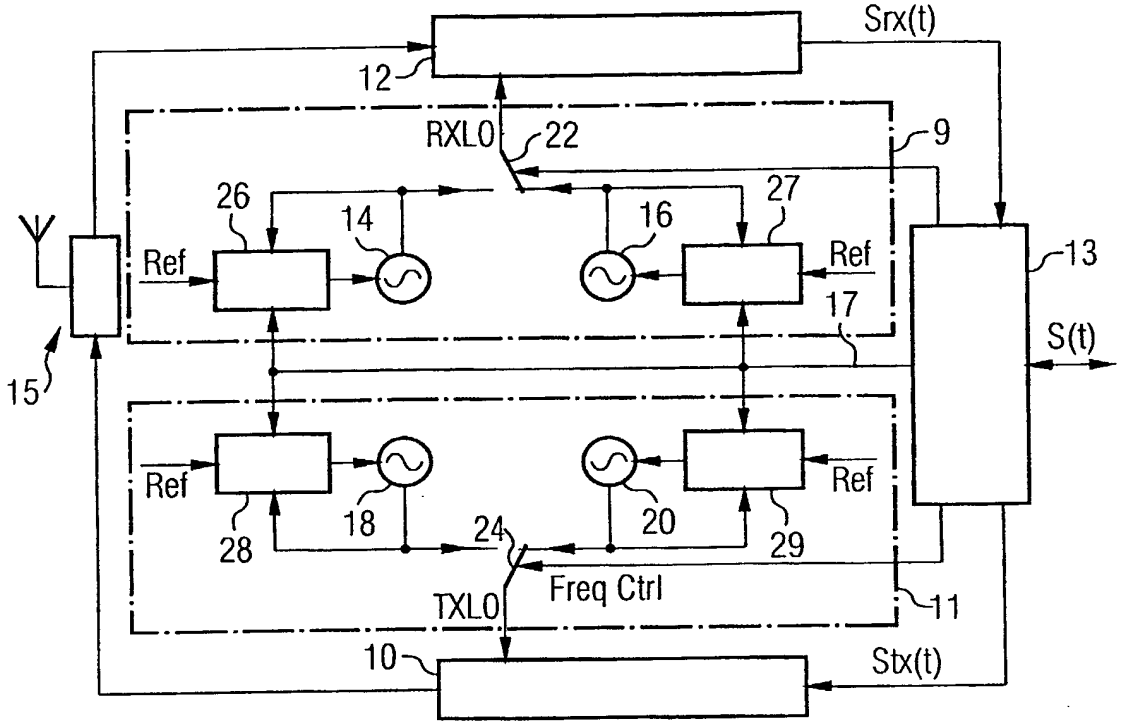

Srx(t)
12
RXLO
22
9
26
14
16
27
Ref
Ref
13
17
S(t)
15
Ref
Ref
28
18
24
20
29
Freq Ctrl
TXLO
11
10
Stx(t)

FIG 2

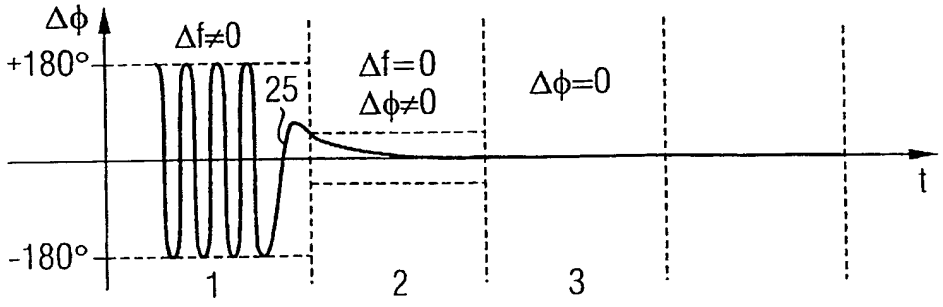

Δϕ
Δf≠0
+180°
25
Δf=0
Δϕ≠0
Δϕ=0
t
-180°
1
2
3

FIG 3

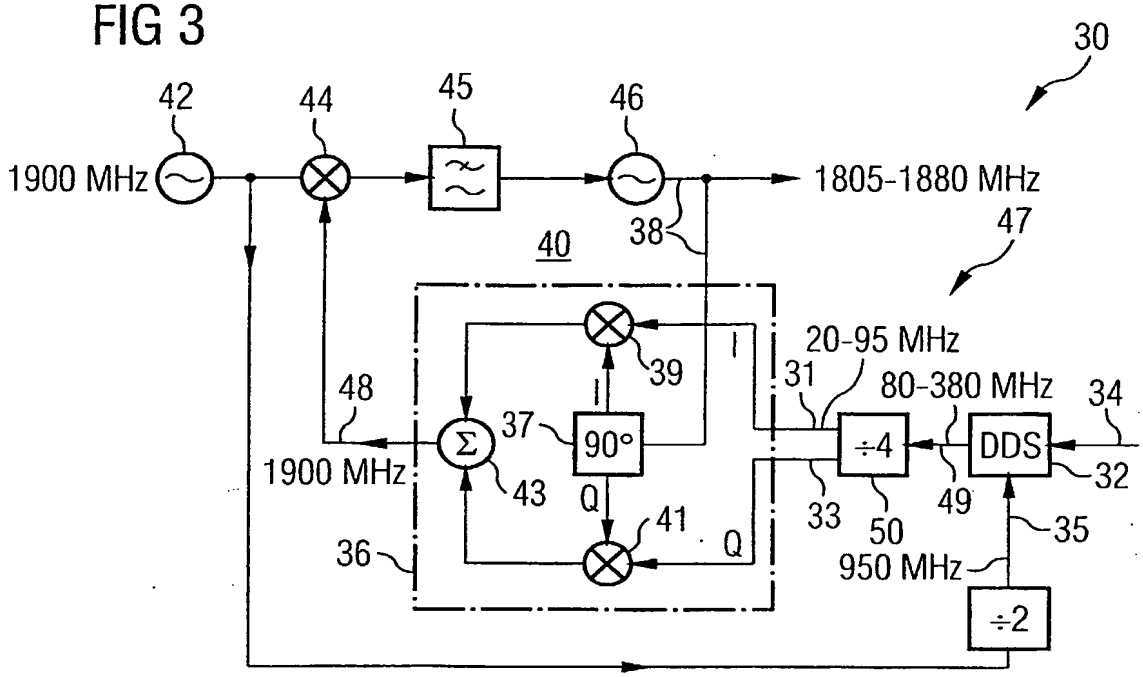

30
42
44
45
46
1900 MHz
1805-1880 MHz
38
47
40
39
I
20-95 MHz
31
80-380 MHz
34
48
37
90°
÷4
DDS
1900 MHz
43
Q
41
Q
33
50
49
32
35
36
950 MHz
÷2

FIG 4

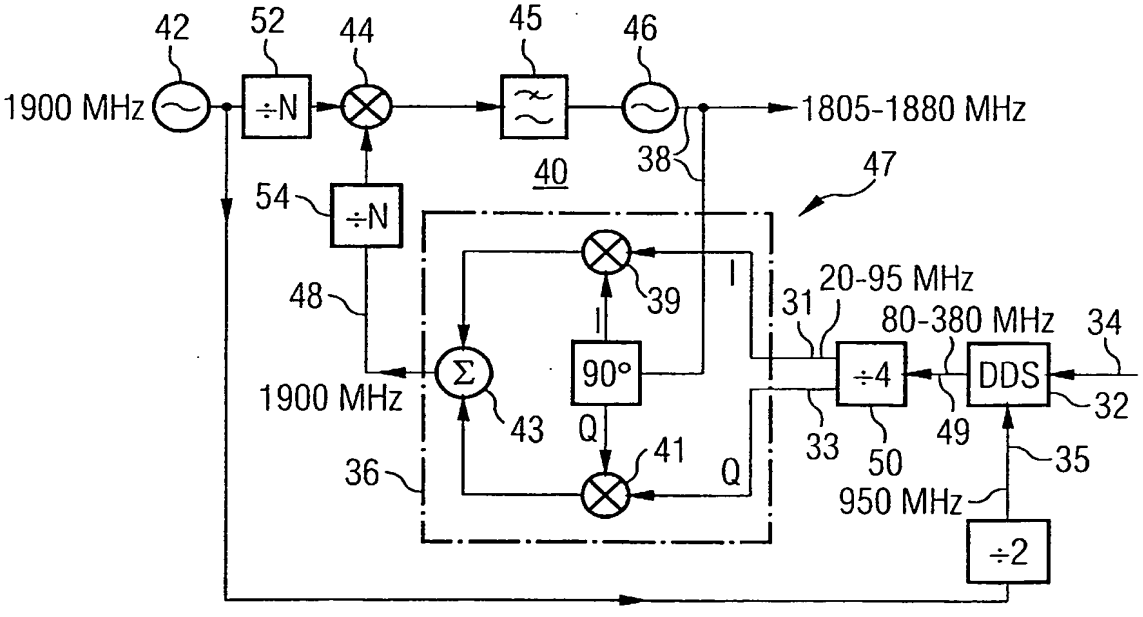

42
52
44
45
46
1900 MHz
÷N
1805-1880 MHz
38
40
47
54
÷N
39
I
48
20-95 MHz
31
80-380 MHz
34
37
90°
÷4
DDS
1900 MHz
43
Q
41
Q
33
50
49
32
35
36
950 MHz
÷2

FIG 5

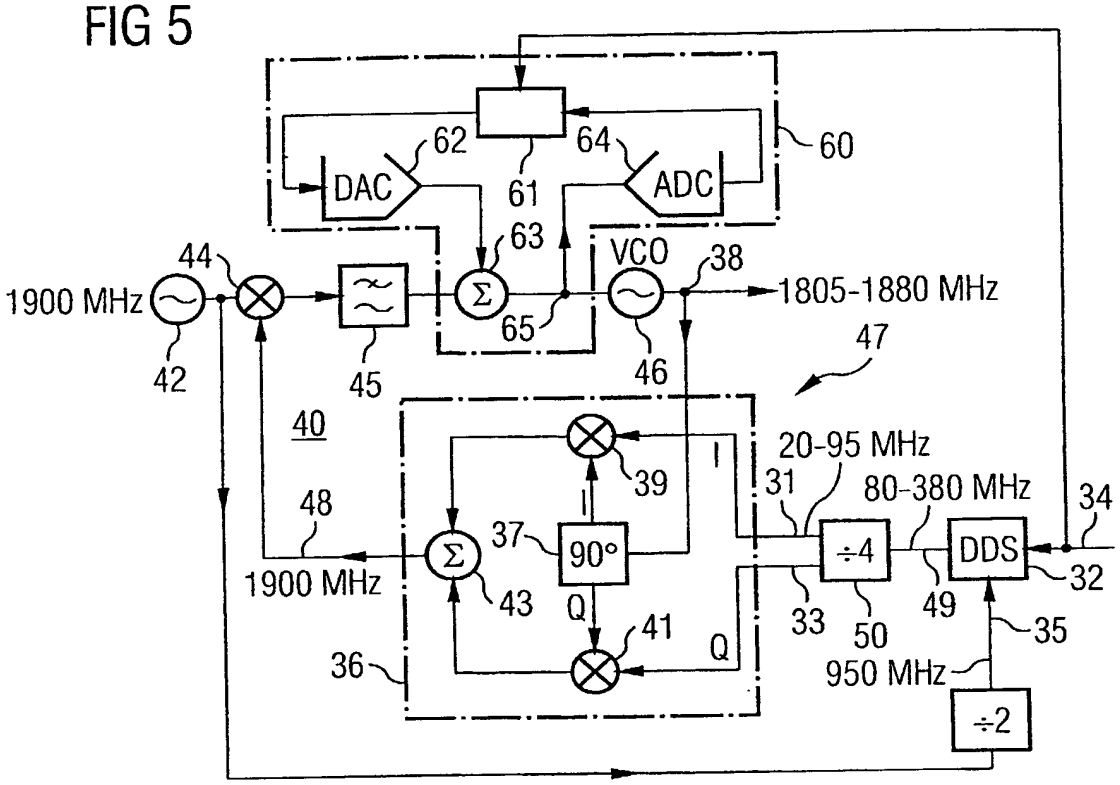

60
62
64
DAC
61
ADC
63
VCO
38
44
1900 MHz
1805-1880 MHz
65
42
45
46
47
40
20-95 MHz
39
31
80-380 MHz
34
48
37
90°
÷4
DDS
Σ
43
Q
41
Q
33
50
49
32
1900 MHz
36
35
950 MHz
÷2

FIG 6

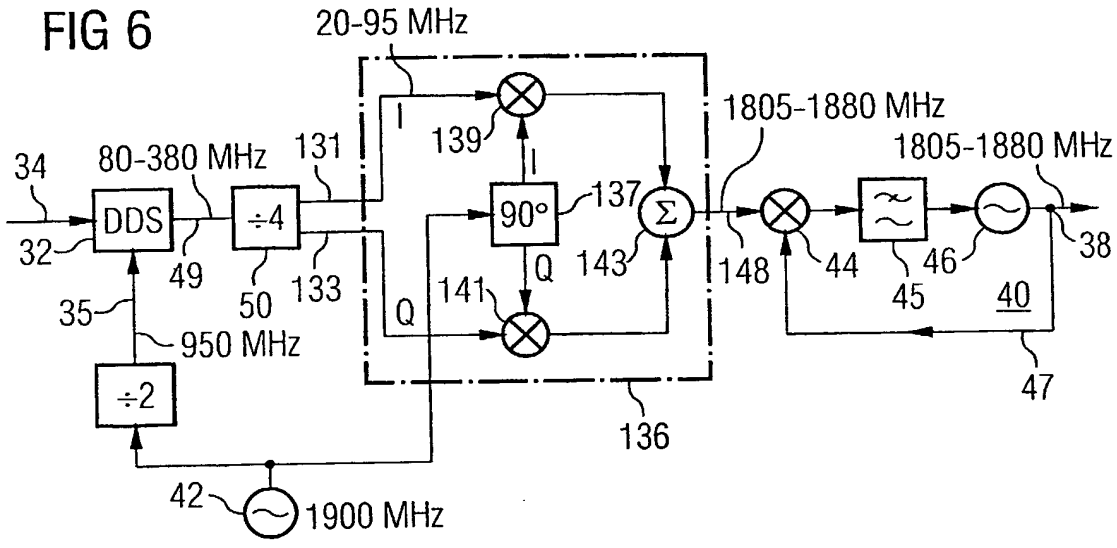

20-95 MHz
I
139
1805-1880 MHz
1805-1880 MHz
34
80-380 MHz
131
137
Σ
DDS
÷4
90°
Q
143
148
44
46
38
32
49
50
133
141
Q
45
40
35
950 MHz
÷2
47
136
42
1900 MHz

FIG 7

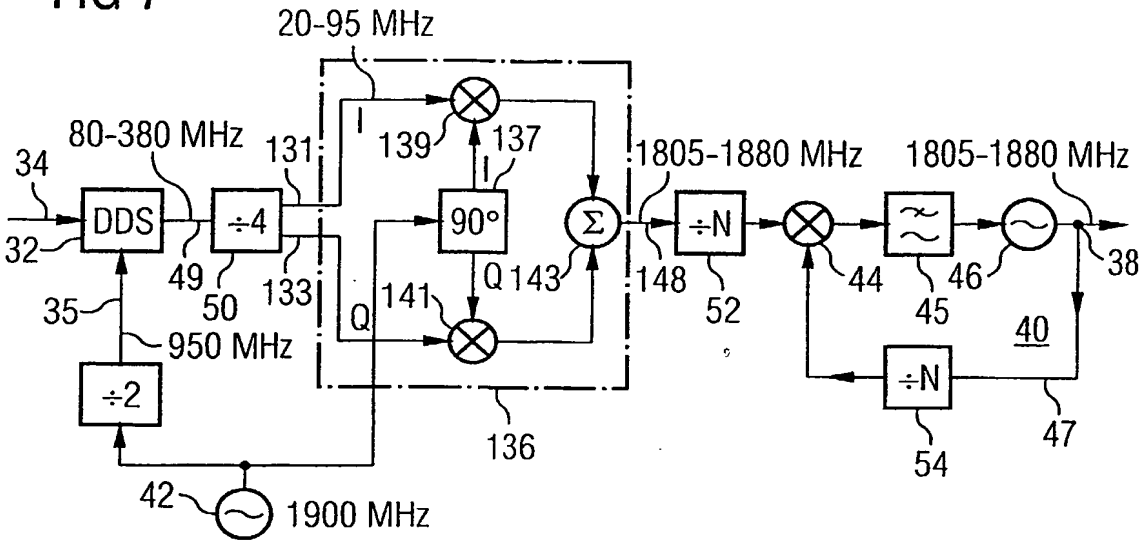
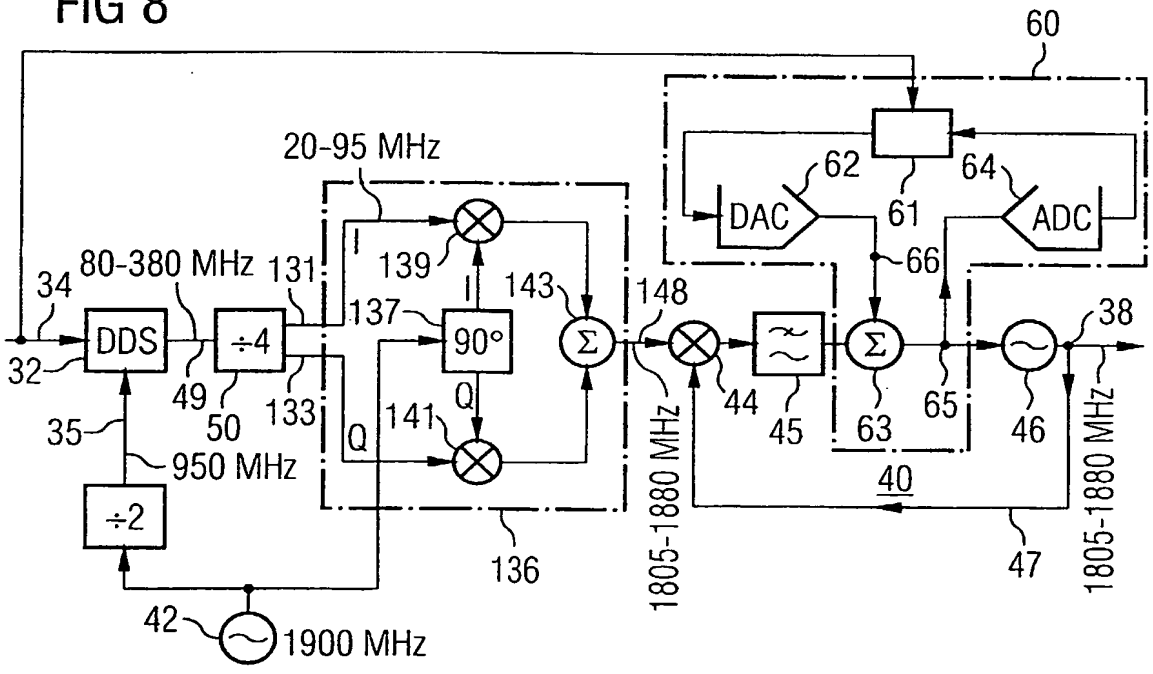

20-95 MHz
80-380 MHz
131
139
137
1805-1880 MHz
1805-1880 MHz
34
DDS
÷4
90°
Σ
÷N
32
49
50
133
Q
141
Q
143
148
52
44
46
45
38
35
950 MHz
40
÷N
÷2
136
47
54
42
1900 MHz

FIG 8


60
20-95 MHz
62
64
DAC
61
ADC
66
80-380 MHz
131
139
143
148
34
DDS
÷4
137
90°
Σ
38
32
49
50
133
Q
141
Q
44
45
63
65
46
35
950 MHz
40
÷2
136
1805-1880 MHz
47
1805-1880 MHz
42
1900 MHz

IMPROVEMENTS IN OR RELATING TO FAST FREQUENCY-HOPPING SYNTHESISERS

The present invention relates to frequency hopping synthesisers. More particularly, it relates to low-noise, fast hopping synthesisers for use in local oscillators for base stations of mobile telephone networks.

In base station transceivers used in GSM/EDGE mobile telephone networks, frequency-hopping synthesisers are required which have high switching speed, low phase noise and low spurious components simultaneously. The phase noise is important, as the baseband signal is encoded on to the RF carrier by phase modulation. In a typical carrier unit, 2-4μs transmit switching speed is necessary, typically with a signal-to-spurious frequency performance of better than –80dBc.

A known Carrier Unit (CU) for use in a mobile telephone base station is shown in Fig. 1. As shown, a transmit path 10 and a receive path 12 each communicate between a baseband processor and controller 13 and a radio transceiver 15. The transmit path 10 and receive path 12 each require a respective local oscillator signal TXLO, RXLO from a respective local oscillator 9, 11. Four separate independent synthesisers 14, 16, 18, 20 are used for this purpose, which are switched from slot to slot in a 'leap-frog' configuration. That is, while one synthesiser (e.g. 14) is in use, its complementary synthesiser 16 is tuning to the required frequency for the next slot. When the next slot begins, switch 22 will pass the output of 16 as the signal RXLO, and the synthesiser 14 will then begin tuning to the frequency of the following slot. The synthesisers 18, 20 of the transmit path operate similarly. The baseband processor and controller 13 sends frequency control signals 17 to each of the synthesisers, and a reference frequency Ref is also applied to each synthesiser.

The solution of Fig.1 is expensive because it requires four voltage controlled oscillators 14, 16, 18, 20, four synthesisers 26, 27, 28, 29, two RF switches 22, 24 and the associated control circuitry. Furthermore, all of these components must be housed in separately screened compartments to minimise interference between the

signal generated by each synthesiser. The interference may be particularly troublesome when one synthesiser is tuning between frequencies and happens to cross the frequency at which a neighbouring synthesiser is operating.

Known solutions exist, having only one voltage controlled oscillator and one synthesiser for each local oscillator 9, 11. For example, such solutions include those known as DDS (Direct Digital Synthesis) and fractional-N solutions. However, neither DDS nor fractional-N meet both the switching speed requirements and the spectral purity requirements for GSM simultaneously.

The present invention accordingly aims to provide a carrier unit of reduced complexity, having only one voltage controlled oscillator and one synthesiser for each local oscillator 9, 11 which provides enhanced performance of the DDS solution in terms of spectral purity and, according to certain embodiments, also in improved switching speed.

The invention further aims to provide a single-chip solution for the GSM hopping synthesiser, employing such a carrier unit.

The present invention accordingly provides a low noise fast frequency-hopping local oscillator for use in a base station for a mobile telephone network. A low noise hopping frequency is provided by a combination of a fast direct digital synthesis (DDS) circuit feeding a frequency divider. A vector modulator and phase locked loop act together to translate the hopping frequency from a relatively low frequency range to a required RF frequency range.

The present invention accordingly provides a low noise fast frequency-hopping oscillator comprising: a combination of a direct digital synthesis (DDS) circuit and a frequency divider, in which the DDS circuit provides a synthesised signal to a frequency divider which itself provides a hopping frequency as a predetermined submultiple of the output frequency of the DDS circuit; and a combination of

a reference frequency oscillator, a vector modulator and phase locked loop, which combination translates the hopping frequency from a relatively low frequency to a required output frequency of the local oscillator, as the difference between an output frequency of the reference frequency oscillator and the hopping frequency.

The reference frequency oscillator preferably supplies a reference frequency to a first input of a phase comparator of the phase locked loop. A feedback path of the phase locked loop preferably comprises the vector modulator and the combination of the DDS circuit and the divider, acting to supply a frequency equal to the reference frequency to a second input of the phase comparator. A voltage controlled oscillator ("vco") of the phase locked loop preferably supplies the required frequency.

Alternatively, the reference frequency oscillator may supply a reference frequency to a first input of the vector modulator. In this case the combination of the DDS circuit and the divider may act to supply a hopping frequency to further inputs of the vector modulator. The vector modulator may then supply a frequency equal to the required frequency to the phase locked loop comprising a phase comparator, a loop filter and a vco, the phase locked loop being arranged to act as a frequency tracking filter.

The DDS circuit may be arranged to receive a clock signal supplied via a frequency divider from the reference frequency oscillator.

The oscillator may further comprise a frequency divider at each input of the phase comparator, whereby the phase comparator is arranged to operate at a submultiple of the frequency of each input signal.

The phase locked loop may further comprise a pretuning block to provide a predetermined control voltage to the vco in response to selection of a required output frequency of the local oscillator. The pretuning block may be self-calibrating. In particular, the pretuning block may comprise a memory receiving

frequency commands; a digital to analogue converter for receiving signals from memory representing a control voltage to be applied to the vco and an analogue to digital converter for supplying a digital representation of the control voltage applied to the vco, the memory being arranged to store such digital representation in a location corresponding to the applied frequency commands.

The present invention also provides a carrier unit for a mobile telephone base station comprising: a radio transceiver; transmit and receive local oscillators; a transmit path arranged to supply RF signals to the radio receiver, and to receive a transmit local oscillator signal from the transmit local oscillator; a receive path arranged to receive RF signals from the radio transceiver and to receive a receive local oscillator signal from the receive local oscillator; and a baseband processor and controller providing control signals to the transmit and receive local oscillators and for supplying a baseband signal to the transmit path and receiving a baseband signal from the receive path, wherein at least one of the transmit and receive oscillators is as described above.

The present invention also provides a mobile telephone base station comprising a carrier unit as described above.

The present invention also provides a method of providing a low-noise fast frequency-hopping RF signal, comprising the steps of: operating a digital direct synthesiser (DDS) to produce an output frequency at a predetermined multiple N of a hopping frequency; frequency dividing the output of the DDS by the predetermined multiple N, to produce a hopping frequency; and frequency translating the hopping frequency to achieve the required frequency by generating a frequency equal to the difference between the hopping frequency and a fixed reference frequency.

The method may further comprise the step of filtering the required frequency in a tracking filter.

The method may further comprise the step of pre-tuning the tracking filter.

The above, and further, objects, characteristics and advantages of the present invention will become more apparent with reference to the following description of certain embodiments, given by way of examples only, in conjunction with the accompanying drawings, in which:

Fig. 1 shows a known architecture of carrier unit for a hopping transceiver in a base station for a mobile telephone network;

Fig. 2 shows the phase error of an output of a local oscillator in a frequency hopping carrier unit, acquiring a required frequency and phase;

Fig. 3 shows a local oscillator according to a first embodiment of the present invention;

Fig. 4 shows a local oscillator according to a second embodiment of the present invention;

Fig. 5 shows a local oscillator according to a third embodiment of the present invention;

Fig. 6 shows a local oscillator according to a fourth embodiment of the present invention;

Fig. 7 shows a local oscillator according to a fifth embodiment of the present invention; and

Fig. 8 shows a local oscillator according to a sixth embodiment of the present invention.

Before describing the present invention in detail, reference is made to Fig. 2 which shows the phase error $\Delta\phi$ in an output signal of a voltage controlled oscillator being tuned to a required frequency and phase, in a local oscillator of a frequency-hopping carrier unit. Fig.2 also represents a typical output of the phase comparator of any of the following embodiments of the present invention.

In the first region, labelled 1, the voltage controlled oscillator is oscillating at a different frequency from the required or reference frequency, that is, $\Delta f \neq 0$. Cyclic phase errors reaching $\pm 180°$ are seen, representing a beat frequency being the difference between the reference frequency and the frequency generated by the voltage controlled oscillator. As the voltage controlled oscillator is controlled to reach the required frequency, the beat frequency slows down and eventually, at the end of the first region, a final zero crossing 25 occurs. The vco is providing the required frequency and $\Delta f=0$. There is, however, still a phase error $\Delta\phi \neq 0$ between the vco output and the reference signal.

During a second region, labelled "2" in Figure 2, operation of the local oscillator draws the phase of the vco signal ever closer to the phase required to synchronise the phases of the reference signal and the feedback signal, respectively applied to the inputs of the phase comparator of the local oscillator of the present invention, as discussed in more detail below, progressively reducing $\Delta\phi$.

By the end of the second phase, the vco output signal has been brought into phase with the reference signal and $\Delta\phi=0$.

For a fast frequency hopping transducer, the first and second regions 1, 2 should be made as short as possible, so that the vco signal is ready for use as soon as possible. However, an active burst, i.e. active data transmission or reception, may begin during the second phase 2, while a phase error is still present. This can cause interference with a baseband signal which is phase modulated onto its RF carrier.

Figure 3 shows a local oscillator 30 according to an embodiment of the present invention. In this embodiment, a local oscillator 30 is provided which uses frequency translation to allow a phase locked loop 40 to lock to a fixed reference frequency 42, in this example 1900MHz. A fast 'Digital Direct Synthesis' (DDS) circuit 32, as is commercially available, is used in conjunction with a vector modulator 36. DDS circuit 32 receives a clock signal 35, in this example at 950MHz, and digitally synthesises an output signal at the required frequency. An input signal 34 controls the frequency provided by the DDS circuit. Since a clock signal of 950MHz can be used, frequencies of up to about 400MHz can be synthesised.

Vector modulator 36 receives In-phase (I) and Quadrature (Q) reference signals 31, 33, and an output signal 38. A phase shift element 37 provides In-phase (I) and Quadrature (Q) versions of the output signal 38 to respective phase comparators 39, 41. The outputs of these phase comparators are summed by a summing circuit 43 to produce at output signal at a frequency which is equal to the sum of the frequencies of the reference signals 31, 33 and the frequency of the output signal 38.

Operation of the whole local oscillator 30, according to the first embodiment of the present invention, will now be described. A fixed reference frequency (1900MHz) is supplied by oscillator 42 to one input of a phase comparator 44. The output of phase comparator 44 is applied to a low-pass loop filter 45, whose output controls a vco 46 to provide the required output signal 38. Phase locked loop 40 consists of phase comparator 44, loop filter 45 and vco 46 together with a feedback path 47 which will now be described in more detail.

In the example shown, the output frequency may be required to vary in the range 1805-1880MHz. The frequency of the fixed reference frequency may suitably be chosen as slightly higher than the maximum output frequency that may be desired. In the present case, the fixed reference frequency may be 1900MHz.

Vector modulator 36 is present in the feedback path 47 for providing frequency translation. Since the output frequency 48 of the vector modulator is equal to the sum of the frequency of the vco output signal 38 and the frequency of the reference signals 31, 33, then the frequency of the vco output is controlled by setting the frequency of signals 31, 33 to the difference between the reference frequency of 42 and the required vco output frequency 38, according to control signals 34. In this example, this difference frequency will vary between 20 and 95MHz to provide vco output frequencies of 1805-1880MHz. The difference frequency may alternatively be referred to as a hopping frequency, as this is the frequency which will be changed when a frequency hop is required, which will be translated to the final output frequency by vector modulator 36 and phase locked loop 40.

There are of course many ways to provide a frequency of between 20 and 95MHz. However, the present invention uses a high speed DDS circuit followed by a frequency divider, which has various particular technical benefits, as will be described below. DDS circuit 32 receives a clock signal 34 at a relatively high frequency such as 950MHz. This clock signal 34 may be conveniently provided from fixed reference frequency 42, by dividing by 2 in this case. The DDS circuit is preferably operated over most of its range, in this example, producing output frequencies of 80-380MHz. As is a known feature of DDS circuits, along with the required frequency, various 'spurious' frequencies are also produced at a lower level. The ratio between the magnitude of the required frequency and the spurious frequencies as produced by the DDS is important in determining how difficult it will be to filter out unwanted frequencies in the output signal.

According to an aspect of the invention, the output signal 49 from the DDS circuit is frequency divided by a divider 50. In this example, the divider 50 divides the frequency of signal 49 by 4. This has at least two advantages. Firstly, by taking outputs at different phases from within the divider, it is easy to obtain the In-phase (I) and Quadrature (Q) signals required for the vector modulator 36. Furthermore, the ratio of magnitudes of the required frequency to spurious frequencies is improved by 12dB. This is in marked contrast to certain prior art systems which

multiply the output of the DDS to provide the output signal 38. A major problem with this is that the ratio of magnitudes between the required frequency and the spurious frequencies is degraded. For example, doubling the output frequency of the DDS may be expected to degrade the ration of magnitudes by 6dB.

Accordingly, the divider 50 provides low noise in-phase and quadrature signals 31, 33 at a frequency equal to the difference between the fixed frequency reference (1900MHz) and the required output frequency 38. For example, if an output frequency of 1805MHz is required, the DDS circuit is controlled to provide a frequency of 380 MHz, which is divided by the divider 50 into in-phase and quadrature signals at 95MHz. The vector modulator 36 performs a translation and provides an output signal 48 representing the frequency sum of the 95MHz signal and the output signal 38 at its prevailing frequency. This signal 48 will be compared to the fixed reference frequency by the phase comparator 44. The phase comparator 44 and loop filter 45 will control the vco 46 to adjust its output signal 38 in frequency such that the signal 48 will have a frequency equal and in phase with the fixed frequency reference 42. The output signal 38 will then be fixed at 1805 MHz, as required.

The output signal 48 of the vector modulator 36 will in practice contain a small residue of the vco output frequency 38, as well as an 'image' term equal to the difference between the VCO output frequency 38 and the frequency of signals 31, 33. However, by suitably choosing the natural frequency and damping factor of the phase locked loop 40, for example by appropriately configuring loop filter 45, these unwanted components can be filtered to an acceptably low level.

Fig. 4 shows a local oscillator according to a second embodiment of the present invention. Features corresponding to features of the embodiment of Fig. 3 carry corresponding reference numerals. In Fig. 4, corresponding frequency dividers 52, 54 are provided in each input to the phase comparator 44. This embodiment has the advantage of reducing the input frequency requirements of the phase comparator, enabling a slower, simpler and therefore lower-cost phase comparator to be used.

With this embodiment, the resulting noise level in the output signal 38 may be higher as a result of the inclusion of dividers 52, 54. Preferably, each divider divides by the same factor, N. It is possible, however, to use different divisors N in the two dividers 52, 54, by appropriate selection of the frequency of the fixed reference frequency 42.

The embodiment of Fig. 3 may be seen as a special case of the embodiment of Fig. 4, where N is set to 1 in each of the dividers 52, 54.

Fig. 5 shows a third embodiment of the local oscillator according to the present invention. Features corresponding to features of the embodiments of Figs. 3 and 4 carry corresponding reference numerals.

In this embodiment, a pre-tuning block 60 is added, located in the forward path of phase locked loop 40 between the loop filter 45 and the vco 46. The pre-tuning block comprises a memory 61, a digital-to-analogue converter (DAC) 62, a summer 63 and an analogue-to-digital converter 64. The pre-tuning block is intended to reduce the duration of the first stage 1 of the tuning process, as illustrated in Fig. 2. Memory 61 contains a digital value corresponding to a previous value applied to vco 46 in order to achieve the required output frequency, as indicated by signal 34, which is additionally supplied to the memory 61 acting as a look-up table.

In this arrangement a stored pre-tuning voltage 66 is applied to the vco control input, which forces the vco 46 close to the desired new frequency each time a frequency hop is required.

The values stored in memory 61 are periodically updated by monitoring the control voltage 65 at the vco input once the loop has settled to a steady state value. ADC 64 digitises this input voltage and provides the digitised representation to memory 61 which stores it in place of the previously stored value for that required frequency.

Normal phase locked loop operation pulls the frequency of the vco into lock with the fixed input reference frequency 42, through second and third regions, 2 and 3 of Fig. 2. The control voltage applied to the vco is a sum of the voltage of signal 66 and the output of loop filter 45. In the absence of drift the output of loop filter 45 would settle to zero when the required frequency and phase were obtained. However, drift is likely in the various parameters of the phase locked loop 40, and an output voltage will be produced at the output of loop filter 45 when the required frequency and phase have been obtained to compensate for this drift. The value at vco input 65 is then stored in memory 61 for use at a next hop to the same required frequency.

When a frequency hop is required, signals 34 indicating the required frequency are applied to the DDS circuit 32 and the memory 61. The DDS provides a synthesised 'hopping' frequency for use as described with reference to Fig. 3. Memory 61 uses signals 34 to retrieve from memory a value representing the input 65 to the vco which provided the corresponding required output frequency when it was last used. This value is supplied to DAC 62, which converts it into an analogue voltage 66 which is applied to the input of vco 46. This forces the vco 46 to operate at a frequency very close to the desired frequency, placing operation of the local oscillator at a point near the end of region 1 of Fig. 2. Normal phase locked loop operation pulls the frequency of the vco into lock with the fixed input reference frequency 42, through second and third regions, 2 and 3 of Fig. 2. The control voltage applied to the vco is a sum of the voltage of signal 66 and the output of loop filter 45. In the absence of drift, the output of loop filter 45 would settle to zero when the required frequency and phase were obtained. However, drift is likely in the various parameters of the phase locked loop 40, and an output voltage will be produced at the output of loop filter 45 when the required frequency and phase have been obtained, to compensate for this drift. The value at vco input 65 is then stored in memory 61 for use at a next hop to that same required frequency. Depending on the initial difference between the required frequency and the previous operating frequency of the vco 46, the first region 1 may otherwise be relatively long, and the pretuning according to this embodiment of the invention may be used to

considerably shorten the time required for the local oscillator to acquire the required frequency and phase.

Once the frequency of the vco has settled into the required frequency and phase, the voltage then present at the input of the vco is stored in memory 61, as a digital representation supplied by ADC 64, in a location corresponding to the required frequency, so that next time the same required frequency is indicated by signals 34, the most recently used vco control voltage is applied to the vco input 65, to allow the required frequency and phase to be attained in as short a time as possible. Since each channel, that is, frequency, is typically used every few milliseconds in a typical mobile telephone network, this self-calibration method allows various forms of drift to be accurately compensated for, and provides a minimum tuning time.

This method will, of course, only operate properly once each frequency has been used once. The memory 61 may initially be loaded with typical values for the vco input for each respective frequency, or a long set up time must be tolerated for each frequency the first time it is used.

Fig. 6 shows a fourth embodiment of the present invention. Features common with the embodiments of Figs. 1-5 carry corresponding reference numerals. In this embodiment, the DDS circuit 32, the divider 50 and a vector modulator 136 are all located in the input path of the phase locked loop 40 and provide the required frequency at the output 48 of the vector modulator 136, with the phase locked loop itself tracking the input frequency from the vector modulator and acting as a filter.

Vector modulator 136 receives In-phase (I) and Quadrature (Q) reference signals 131, 133 and reference signal 42. A phase shift element 137 provides In-phase (I) and Quadrature (Q) versions of the reference signal 42 to respective phase comparators 139, 141. The outputs of these phase comparators are summed by a summing circuit 143 to produce at output signal at a frequency which is equal to the sum of the frequencies of the reference signals 131, 133 and the frequency of the output signal 138.

As with previous embodiments, to produce a final output frequency 38 of 1805-1880MHz, DDS circuit 32 and divider 50 are used to provide in-phase (I) and quadrature (Q) signals at a frequency equal to the difference between the fixed reference frequency 42 and the required output frequency. For example, to produce an output of 1805MHz, the output of divider 50 needs to be at 95(=1900-1805) MHz. This may be produced by using a 380MHz signal from the DDS circuit and dividing by 4 in the divider 50. By taking signals from different phases within the divider, in-phase (I) and quadrature (Q) signals 131, 133 may be easily provided. As in earlier embodiments, the clock signal for the DDS circuit may be conveniently supplied by the fixed frequency reference 42, in this example by dividing the 1900 MHz reference signal by 2. Vector modulator 136 is supplied with reference frequency 42 into its phase shift element 137, which produces in-phase (I) and quadrature (Q) versions of the signal to the phase comparators 139, 141.

Unlike the embodiments shown in Figs. 3-5, the vector modulator 136 of this embodiment here performs a translation operation which results in the production of a frequency equal to the difference of the input frequencies, rather than the sum of the input frequencies, as was the case in the embodiments of Figs. 3-5.

In this embodiment, the vector modulator 136 is producing the output frequency (1805-1880 MHz), whereas in the embodiments described above, the vector modulator 36 was producing a fixed offset frequency (1900 MHz).

It will be apparent to one skilled in the art that vector modulators may be arranged to provide output frequencies equal to a sum and/or a difference of input frequencies, as required.

Accordingly, the summer 143 essentially provides an output signal 148 of 1805MHz, in the present example. While this signal has the required frequency and phase, it contains spurious frequencies generated by the DDS circuit 32. As

discussed with reference to Fig. 3, these spurious signals are greatly reduced in magnitude as compared to the output signal of the DDS, by use of the divider 50. The level of the spurious frequencies is even further reduced as compared with prior art methods which employ a multiplier at the output of the DDS circuit.

The output of the vector modulator 136 will also contain some residual signal at the fixed reference frequency, 1900MHz in this case, and at an image frequency equal to the fixed reference frequency plus the frequency of the output of the divider 50, 95 MHz in this case, giving an image frequency component of 1995MHz.

Each of these image or residual signals will be separated from the required frequency by a substantial frequency offset – at least 20MHz in this example for the residual fixed frequency, and at least 40MHz for the image frequency. It is therefore a relatively simple matter to filter out these signals by suitably choosing the loop parameters of the phase locked loop 40, such as the characteristics of the loop filter 45. A loop filter 45 with a pass bandwidth of 1-5MHz will be relatively simple to implement, and sufficient to filter out the unwanted frequencies at a frequency separation of at least 20MHz. The loop filter will also filter out much of the remaining spurious frequency signals produced by the DDS and divider 32, 50.

Fig. 7 shows a fifth embodiment of the present invention. Features common with the embodiments of Figs 1-6 carry corresponding reference numerals. The embodiment of Fig. 7 differs from that of Fig. 6 only in that corresponding frequency dividers 52, 54 are provided in each input to the phase comparator 44. This embodiment has the advantage of reducing the input frequency requirements of the phase comparator 44, enabling a slower, simpler and therefore lower-cost phase comparator to be used. With this embodiment, the resulting noise level in the output signal 38 may be higher as a result of the inclusion of dividers 52, 54. Preferably, each divider divides by the same factor, N. It is possible, however, to use different divisors N in the two dividers 52, 54, by appropriate selection of the frequency of the fixed reference frequency 42.

The embodiment of Fig. 6 may be seen as a special case of the embodiment of Fig. 7, in which N is set to 1 in each of the dividers 52, 54.

Fig. 8 shows a sixth embodiment of the local oscillator according to the present invention. Features corresponding to features of the embodiments of Figs. 3-7 carry corresponding reference numerals.

In this embodiment, a pre-tuning block 60 is added, located in the forward path of phase locked loop 40 between the loop filter 45 and the vco 46. The pre-tuning block comprises a memory 61, a digital-to-analogue converter (DAC) 62, a summer 63 and an analogue-to-digital converter 64. The pre-tuning block is intended to reduce the duration of the first stage 1 of the tuning process, as illustrated in Fig. 2. Memory 61 contains a digital value corresponding to a previous value of control signal 65 applied to vco 46 in order to achieve the required output frequency, as indicated by signal 34, which is additionally supplied to the memory 61 acting as a look-up table.

In this arrangement a stored pre-tuning voltage 66 is applied to the vco control input 65, which forces the vco 46 close to the desired new frequency each time a frequency hop is required.

The values stored in memory 61 are periodically updated by monitoring the control voltage 65 at the vco input once the loop has settled to a steady state value. ADC 64 digitises this input voltage and provides the digitised representation to memory 61 which stores it in place of the previously stored value for that required frequency.

When a frequency hop is required, signals 34 indicating the required frequency are applied to the DDS circuit 32 and the memory 61. The DDS provides a synthesised frequency for use as described with reference to Fig. 6. Memory 61 uses signals 34 to retrieve from memory a value representing the input to the vco which provided the corresponding output frequency when it was last used. This value is supplied to

DAC 62, which converts it into an analogue voltage which is applied to the input of vco 46. This forces vco 46 to operate at a frequency very close to the desired frequency, placing operation of the local oscillator at a point near the end of region 1 of Fig. 2. The control voltage applied to the vco is a sum of the voltage of signal 66 and the output of loop filter 45. In the absence of drift, the output of loop filter 45 would settle to zero when the required frequency and phase were obtained. However, drift is likely in the various parameters of the phase locked loop 40, and an output voltage will be produced at the output of loop filter 45 when the required frequency and phase have been obtained, to compensate for this drift. The value at vco input 65 is then stored in memory 61 for use at a next hop to that same required frequency. Depending on the initial difference between the required frequency and the previous operating frequency of the vco, the first region 1 may be relatively long, and the pretuning according to this embodiment of the invention may be used to considerably shorten the time required for the local oscillator to acquire the required frequency and phase.

Once the frequency of the vco has settled into the required frequency and phase, the voltage then present at the input of the vco is stored in memory 61, as a digital representation supplied by ADC 64, in a location corresponding to the required frequency, so that next time the same required frequency is indicated by signals 34, the most recently used vco control voltage is applied to the vco input 65, to allow the required frequency and phase to be attained in as short a time as possible. Since each channel, that is, frequency, is typically used every few milliseconds in a typical mobile telephone network, this self-calibration method allows various forms of drift to be accurately compensated for, and provides a minimum tuning time.

This method will, of course, only operate properly after each frequency has been used, at least once. The memory 61 may initially be loaded with typical values for the vco input for each respective frequency, or a long set up time must be tolerated for each frequency the first time it is used.

The present invention accordingly provides a low noise fast frequency-hopping local oscillator for use in a base station for a mobile telephone network, in which a low noise hopping frequency is provided by a combination of a fast direct digital synthesis (DDS) circuit feeding a frequency divider, followed by a vector modulator and phase lockled loop acting together to translate the hopping frequency from a relatively low frequency range to the required RF frequency range for mobile telephone communications.

Any of the local oscillators described according to the present invention may be used in place of the local oscillators 9, 11 shown in the carrier unit (CU) of Fig.1. Present technology allows all elements of the local oscillator other than the loop filter 45 and vco 46, to be integrated into a single integrated circuit ('chip') with the remainder of the carrier unit (CU), thereby substantially providing the sought after one-chip solution.

While the present invention has been described with reference to a limited number of particular embodiments, one skilled in the art will readily appreciate that numerous modifications and variants are possible, within the scope of the present invention. For example, although the invention has been described in terms of a local oscillator for a base station of a mobile telephone network, the present invention may be employed in any situation which requires a fast frequency hopping oscillator. Furthermore, while certain frequency ranges have been discussed with reference to certain examples, the invention is by no means limited to such frequency ranges, and it is anticipated that the present invention will continue to apply to progressively higher frequencies as the capabilities of DDS circuits and frequency dividers improve. The invention equally applied to systems using a lower range of frequencies than that described in the various examples.

CLAIMS

1. A low noise fast frequency-hopping oscillator comprising:
- in combination, a direct digital synthesis (DDS) circuit (32) and a frequency divider (50), in which the DDS circuit provides a synthesised signal (49) to the frequency divider which itself provides a hopping frequency (31,33) as a predetermined submultiple of the output frequency of the DDS circuit; and
- in combination, a reference frequency oscillator (42), a vector modulator (36) and phase locked loop (40), which combination translates the hopping frequency from a relatively low frequency to a required output frequency of the local oscillator, as the difference between an output frequency of the reference frequency oscillator and the hopping frequency.

2. An oscillator according to claim 1 wherein the reference frequency oscillator supplies a reference frequency to a first input of a phase comparator (44) of the phase locked loop, and wherein a feedback path (47) of the phase locked loop comprises the vector modulator and the combination of the DDS circuit and the divider, acting to supply a frequency equal to the reference frequency to a second input of the phase comparator, a voltage controlled oscillator (46) of the phase locked loop supplying the required frequency.

3. An oscillator according to claim 1 wherein the reference frequency oscillator supplies a reference frequency to a first input (37) of the vector modulator, and the combination of the DDS circuit and the divider, acts to supply a hopping frequency to further inputs (39, 41) of the vector modulator, the vector modulator supplying a frequency equal to the required frequency to the phase locked loop comprising a phase comparator (44), a loop filter (45) and a vco (46), the phase locked loop being arranged to act as a frequency tracking filter.

4. An oscillator according to any preceding claim, wherein the DDS circuit is arranged to receive a clock signal supplied via a frequency divider from the reference frequency oscillator.

5. An oscillator according to any of claims 2-4, further comprising a frequency divider (52, 54) at each input of the phase comparator, whereby the phase comparator is arranged to operate at a submultiple of the frequency of each input signal.

6. An oscillator according to any preceding claim wherein the phase locked loop further comprises a pretuning block (61) to provide a predetermined control voltage to the vco (46) in response to selection (34) of a required output frequency of the local oscillator.

7. An oscillator according to claim 6, wherein the pretuning block is self-calibrating.

8. An oscillator according to claim 7 wherein the pretuning block comprises a memory (61) receiving frequency commands (34); digital to analogue converter (62) for receiving signals from memory (61) representing a control voltage (65) to be applied to the vco and an analogue to digital converter (64) for supplying a digital representation of the control voltage applied to the vco, the memory being arranged to store such digital representation in a location corresponding to the applied frequency commands (34).

9. A carrier unit for a mobile telephone base station comprising:

- a radio transceiver (15);
- transmit and receive local oscillators (11, 9);
- a transmit path (10) arranged to supply RF signals to the radio receiver, and to receive a transmit local oscillator signal (TXLO) from the transmit local oscillator (11);
- a receive path (12) arranged to receive RF signals from the radio transceiver and to receive a receive local oscillator signal (RXLO) from the receive local oscillator (9); and

- a baseband processor and controller (13) providing control signals (17) to the transmit and receive local oscillators and for supplying a baseband signal (Stx(t)) to the transmit path and receiving a baseband signal (Srx(t)) from the receive path,

wherein at least one of the transmit and receive oscillators is as claimed in any preceding claim.

10. A mobile telephone base station comprising a carrier unit according to claim 9.

11. A method of providing a low-noise fast frequency-hopping RF signal (38), comprising the steps of:

operating a digital direct synthesiser (DDS) (32) to produce an output frequency (49) at a predetermined multiple N of a hopping frequency;

frequency dividing (50) the output of the DDS by the predetermined multiple N, to produce a hopping frequency (31,33); and

frequency translating the hopping frequency to achieve the required frequency by generating a frequency equal to the difference between the hopping frequency and a fixed reference frequency.

12. A method according to claim 11 further comprising the step of filtering the required frequency in a tracking filter (40).

13. A method according to claim 12 further comprising the step of pre-tuning (61) the tracking filter.

14. A method substantially as described and/or as illustrated in Figs.2-8 of the accompanying drawings.

15. An oscillator substantially as described and/or as illustrated in Figs.2-8 of the accompanying drawings.

Amendments to the claims have been filed as follows

21

CLAIMS

1. A low noise fast frequency-hopping oscillator comprising:
- in combination, a direct digital synthesis (DDS) circuit (32) and a frequency divider (50), in which the DDS circuit provides a synthesised signal (49) to the frequency divider which itself provides a hopping frequency (31,33) as a predetermined submultiple of the output frequency of the DDS circuit; and
- in combination, a reference frequency oscillator (42), a vector modulator (36) and phase locked loop (40), which combination translates the hopping frequency from a relatively low frequency to a required output frequency (38), as the difference between an output frequency of the reference frequency oscillator and the hopping frequency.

2. An oscillator according to claim 1 wherein the reference frequency oscillator supplies a reference frequency to a first input of a phase comparator (44) of the phase locked loop, and wherein a feedback path (47) of the phase locked loop comprises the vector modulator and the combination of the DDS circuit and the divider, acting to supply a frequency equal to the reference frequency to a second input of the phase comparator, a voltage controlled oscillator (46) of the phase locked loop supplying the required frequency.

3. An oscillator according to claim 1 wherein the reference frequency oscillator supplies a reference frequency to a first input (137) of the vector modulator, and the combination of the DDS circuit and the divider, acts to supply a hopping frequency to further inputs (139, 141) of the vector modulator, the vector modulator supplying a frequency equal to the required frequency to the phase locked loop comprising a phase comparator (44), a loop filter (45) and a vco (46), the phase locked loop being arranged to act as a frequency tracking filter.

4. An oscillator according to any preceding claim, wherein the DDS circuit is arranged to receive a clock signal (35) supplied via a frequency divider from the reference frequency oscillator.

5. An oscillator according to any of claims 2-4, further comprising a frequency divider (52, 54) at each input of the phase comparator, whereby the phase comparator is arranged to operate at a submultiple of the frequency of each input signal.

6. An oscillator according to any preceding claim wherein the phase locked loop further comprises a pretuning block (61) to provide a predetermined control voltage to the vco (46) in response to selection (34) of a required output frequency of the local oscillator.

7. An oscillator according to claim 6, wherein the pretuning block is self-calibrating.

8. An oscillator according to claim 7 wherein the pretuning block comprises a memory (61) receiving frequency commands (34); digital to analogue converter (62) for receiving signals from memory (61) representing a control voltage (65) to be applied to the vco and an analogue to digital converter (64) for supplying a digital representation of the control voltage applied to the vco, the memory being arranged to store such digital representation in a location corresponding to the applied frequency commands (34).

9. A carrier unit for a mobile telephone base station comprising:

- a radio transceiver (15);
- transmit and receive local oscillators (11, 9);
- a transmit path (10) arranged to supply RF signals to the radio receiver, and to receive a transmit local oscillator signal (TXLO) from the transmit local oscillator (11);
- a receive path (12) arranged to receive RF signals from the radio transceiver and to receive a receive local oscillator signal (RXLO) from the receive local oscillator (9); and

- a baseband processor and controller (13) providing control signals (17) to the transmit and receive local oscillators and for supplying a baseband signal (Stx(t)) to the transmit path and receiving a baseband signal (Srx(t)) from the receive path,

wherein at least one of the transmit and receive local oscillators is as claimed in any preceding claim.

10. A mobile telephone base station comprising a carrier unit according to claim 9.

11. A method of providing a low-noise fast frequency-hopping RF signal (38), comprising the steps of:

operating a digital direct synthesiser (DDS) (32) to produce an output frequency (49) at a predetermined multiple N of a hopping frequency;

frequency dividing (50) the output of the DDS by the predetermined multiple N, to produce a hopping frequency (31,33); and

frequency translating the hopping frequency to achieve the required frequency by generating a frequency equal to the difference between the hopping frequency and a fixed reference frequency.

12. A method according to claim 11 further comprising the step of filtering the required frequency in a tracking filter (40).

13. A method according to claim 12 further comprising the step of pre-tuning (61) the tracking filter.

14. A method substantially as described and/or as illustrated in Figs.2-8 of the accompanying drawings.

15. An oscillator substantially as described and/or as illustrated in Figs.2-8 of the accompanying drawings.

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): H3A AQA, AQX

Int Cl (Ed.7): H03L 7/18

Other: Online: WPI, EPODOC, PAJ, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2124047 A	(PLESSEY)	
A	GB 2015277 A	(PLESSEY)	
A	US 5311560	(TATSUMI)	

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